NI PXIe-5442 Specifications

16-Bit 100 MS/s Arbitrary Waveform Generator with Onboard Signal Processing (OSP)

このドキュメントには、日本語ページも含まれています。

Unless otherwise noted, the following conditions were used for each specification:

- Analog filter enabled.
- Digital-to-analog converter (DAC) interpolation set to maximum allowed factor for a given sample rate.
- Signals terminated with 50 Ω.
- Direct path set to 1 Vpk-pk, Main path set to 2 V_{pk-pk}.
- Sample clock set to 100 MSamples/s.

Specifications describe the warranted, traceable product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under Specifications or Typical values. Nominal values are not covered by warranty.

Specifications are subject to change without notice. For the most recent NI 5442 specifications, visit `ni.com/manuals`. To access all the NI 5442 documentation, navigate to **Start»All Programs»National Instruments»NI-FGEN»Documentation**.

Caution The protection provided by this product may be impaired if it is used in a manner not described in this document.

Hot Surface If the NI 5442 has been in use, it may exceed safe handling temperatures and cause burns. Allow the NI 5442 to cool before removing it from the chassis.

NATIONAL INSTRUMENTS

Contents

CH 0
(Channel 0 Analog Output, Front Panel Connector)

Specification	Value	Comments
Number of Channels	1	—
Connector	SMB (jack)	—
Output Voltage Characteristics		
Output Paths	1. The software-selectable Main path provides full-scale voltages from 5.64 mVpk-pk to 2.00 Vpk-pk into a 50 Ω load. NI-FGEN uses a low-gain amplifier when you select the Main path. 2. The software-selectable Direct path is optimized for intermediate frequency (IF) applications and provides full-scale voltages from 0.707 to 1.000 Vpk-pk.	—
DAC Resolution	16 bits	—

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td colspan="6">Amplitude and Offset</td></tr>
<tr><td rowspan="8">Amplitude Range</td><td rowspan="2">Path</td><td rowspan="2">Load</td><td colspan="2">Amplitude (Vpk-pk)</td><td rowspan="8">Amplitude values assume the full scale of the DAC is utilized. If you desire an amplitude smaller than the minimum value, you can use waveforms smaller than the full scale of the DAC.
NI-FGEN compensates for user-specified resistive loads.</td></tr>
<tr><td>Minimum Value</td><td>Maximum Value</td></tr>
<tr><td rowspan="3">Direct</td><td>50 Ω</td><td>0.707</td><td>1.00</td></tr>
<tr><td>1 kΩ</td><td>1.35</td><td>1.91</td></tr>
<tr><td>Open</td><td>1.41</td><td>2.00</td></tr>
<tr><td rowspan="3">Main</td><td>50 Ω</td><td>0.00564</td><td>2.00</td></tr>
<tr><td>1 kΩ</td><td>0.0107</td><td>3.81</td></tr>
<tr><td>Open</td><td>0.0113</td><td>4.00</td></tr>
<tr><td>Amplitude Resolution</td><td colspan="4"><0.06% (0.004 dB) of amplitude range</td></tr>
<tr><td>Offset Range</td><td colspan="4">Span of ±25% of amplitude range with increments <0.0014% of amplitude range</td><td>Not available on the Direct path.</td></tr>
<tr><td colspan="6">Maximum Output Voltage</td></tr>
<tr><td rowspan="7">Maximum Output Voltage</td><td>Path</td><td>Load</td><td colspan="2">Maximum Output Voltage (Vpk-pk)</td><td rowspan="7">The maximum output voltage of the NI 5442 is determined by the amplitude range and the offset range.</td></tr>
<tr><td rowspan="3">Direct</td><td>50 Ω</td><td colspan="2">±0.500</td></tr>
<tr><td>1 kΩ</td><td colspan="2">±0.953</td></tr>
<tr><td>Open</td><td colspan="2">±1.000</td></tr>
<tr><td rowspan="3">Main</td><td>50 Ω</td><td colspan="2">±1.000</td></tr>
<tr><td>1 kΩ</td><td colspan="2">±1.905</td></tr>
<tr><td>Open</td><td colspan="2">±2.000</td></tr>
</table>

Specification	Value		Comments
Accuracy			
DC Accuracy	Path		All paths are calibrated for amplitude and gain errors. The Main path is also calibrated for offset errors.
	Main	Direct	
	±0.2% of amplitude ± 0.05% of offset ± 500 µV (within ±10 °C of self-calibration temperature) ±0.4% of amplitude ± 0.05% of offset ± 1 mV (0 to 55 °C)	Gain accuracy: ±0.2% (within ±10 °C of self-calibration temperature) Gain accuracy: ±0.4% (0 to 55 °C) DC error: ±30 mV (0 to 55 °C)	
AC Amplitude Accuracy	(+2.0% + 1 mV), (-1.0% - 1 mV) (+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical		50 kHz sine wave. Signals terminated with high impedance.
Output Characteristics			
Output Impedance	50 Ω nominal or 75 Ω nominal, software-selectable		—
Load Impedance Compensation	Output amplitude is compensated for user-specified load impedances.		—
Output Coupling	DC		—
Output Enable	Software-selectable. When disabled, CH 0 output is terminated with a 1 W resistor with a value equal to the selected output impedance.		—
Maximum Output Overload	The CH 0 output terminal can be connected to a 50 Ω, ±12 V (±8 V for the Direct path) source without sustaining any damage. No damage occurs if CH 0 is shorted to ground indefinitely.		—
Waveform Summing	The CH 0 output terminal supports waveform summing among similar paths—specifically, the outputs of multiple NI 5442 signal generators can be connected together.		—

Specification	Value		Comments
Frequency and Transient Response			
Bandwidth	> 43 MHz		Measured at -3 dB.
DAC Digital Interpolation Filter	Software-selectable finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.		Refer to the *Onboard Signal Processing (OSP)* section for OSP Interpolation information.
Analog Filter	Software-selectable 7-pole elliptical filter for image suppression.		Available only on Main path.
Passband Flatness	Path		With respect to 50 kHz.
	Direct	Main	
	-0.4 to +0.6 dB 100 Hz to 40 MHz	-1.0 to +0.5 dB 100 Hz to 20 MHz	
Pulse Response			
	Path		Analog filter and DAC interpolation filter disabled. All values are typical.
	Direct	Main	
Rise/Fall Time (10 to 90%)	<5 ns <4.5 ns*	<8 ns <5.5 ns*	
Aberration	<12%	<5%	

* Specifications apply only to B-revision and later NI PXIe-5442 devices (National Instruments part number 196749B-0XL).

Figure 1. Normalized Passband Flatness, Direct Path

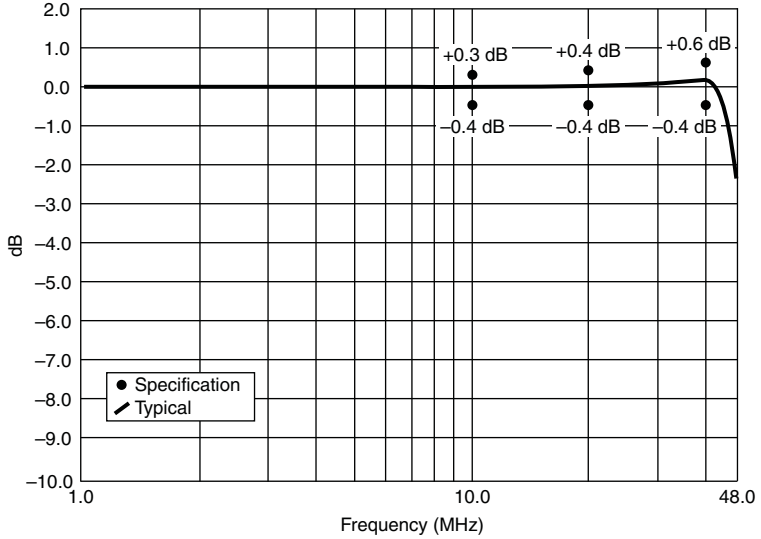


Figure 2. Pulse Response, Main Path with 50 Ω Load (Typical)

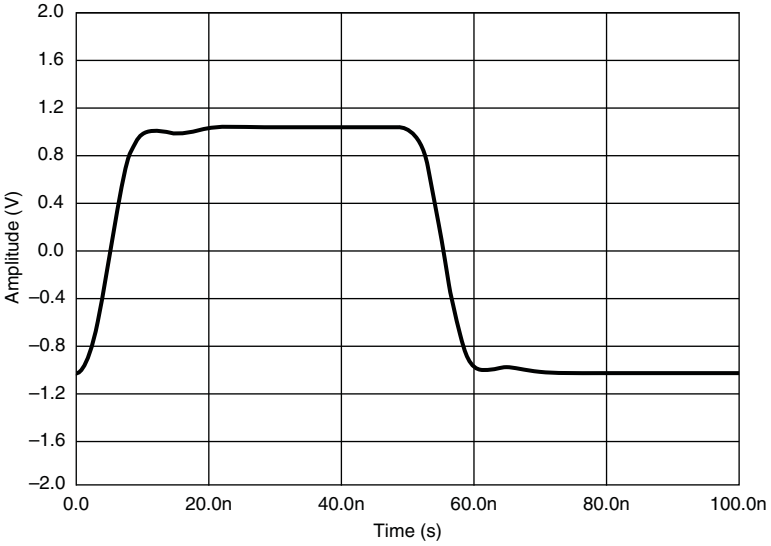
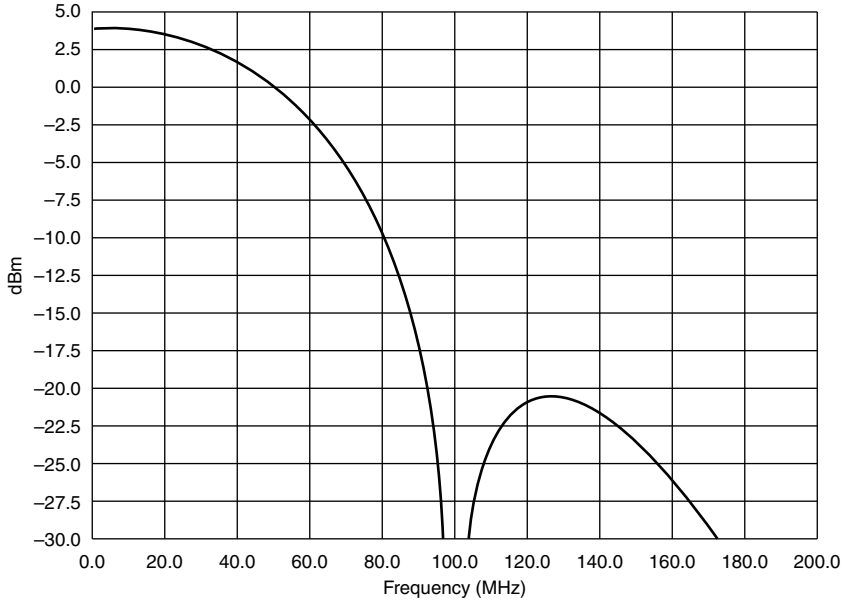


Figure 3. Theoretical Frequency Response of Direct Path, 100 MS/s, 1x DAC Interpolation (Typical)



Note Above 50 MHz, the response is the image response.

Specification	Value		Comments
Suggested Maximum Frequencies for Common Functions			
Function	Path		Disable the Analog filter and the DAC interpolation filter for Ramp and Triangle.
	Direct	Main	
Sine	43 MHz	43 MHz	
Square	Not recommended*	25 MHz	
Ramp	Not recommended*	5 MHz	
Triangle	Not recommended*	5 MHz	
* Direct Path is optimized for the frequency domain.			

Specification	Value		Comments
Spectral Characteristics			
Spurious-Free Dynamic Range* (SFDR) with Harmonics	Path		Amplitude -1 dBFS. Measured from DC to 50 MHz. All values are typical and include aliased harmonics.
	Direct	Main	
1 MHz	76 dB	71 dB	
10 MHz	68 dB	64 dB	
20 MHz	60 dB	57 dB	
30 MHz	73 dB	73 dB	
40 MHz	76 dB	73 dB	
43 MHz	78 dB	75 dB	
* Dynamic range is defined as the difference between the carrier level and the largest spur.			
SFDR without Harmonics	Path		Amplitude -1 dBFS. Measured from DC to 50 MHz. All values are typical and include aliased harmonics.
	Direct	Main	
1 MHz	87 dB	90 dB	
10 MHz	86 dB	88 dB	
20 MHz	79 dB	88 dB	
30 MHz	72 dB	72 dB	
40 MHz	75 dB	72 dB	
43 MHz	77 dB	74 dB	

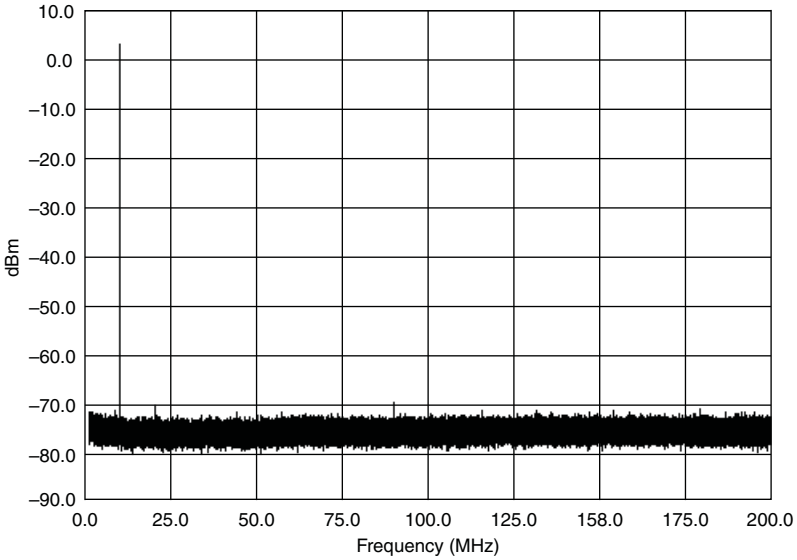
Specification	Value		Comments
Spectral Characteristics (Continued)			
0 to 40 ºC Total Harmonic Distortion (THD)	Path		Amplitude -1 dBFS. Includes the 2nd through the 6th harmonic. All values are typical.
	Direct	Main	
20 kHz	-77 dBc	-77 dBc	
1 MHz	-75 dBc	-70 dBc	
5 MHz	-68 dBc	-68 dBc	
10 MHz	-65 dBc -66 dBc*	-61 dBc -66 dBc*	
20 MHz	-55 dBc -61 dBc*	-53 dBc -61 dBc*	
30 MHz	-50 dBc -57 dBc*	-48 dBc -57 dBc*	
40 MHz	-48 dBc -54 dBc*	-46 dBc -54 dBc*	
43 MHz	-47 dBc -53 dBc*	-45 dBc -53 dBc*	

* Specifications apply only to B-revision and later NI PXIe-5442 devices (National Instruments part number 196749B-0XL).

Specification	Value		Comments
Spectral Characteristics (Continued)			
0 to 55 ºC THD	Path: Direct	Path: Main	Amplitude -1 dBFS. Includes the 2nd through the 6th harmonic. All values are typical.
20 kHz	-76 dBc	-76 dBc	
1 MHz	-74 dBc	-69 dBc	
5 MHz	-67 dBc	-67 dBc	
10 MHz	-63 dBc	-60 dBc	
20 MHz	-54 dBc -57 dBc*	-52 dBc -55 dBc*	
30 MHz	-48 dBc -52 dBc*	-46 dBc -50 dBc*	
40 MHz	-46 dBc -50 dBc*	-41 dBc -47 dBc*	
43 MHz	-45 dBc -49 dBc*	-41 dBc -46 dBc*	
* Specifications apply only to B-revision and later NI PXIe-5442 devices (National Instruments part number 196749B-0XL).			

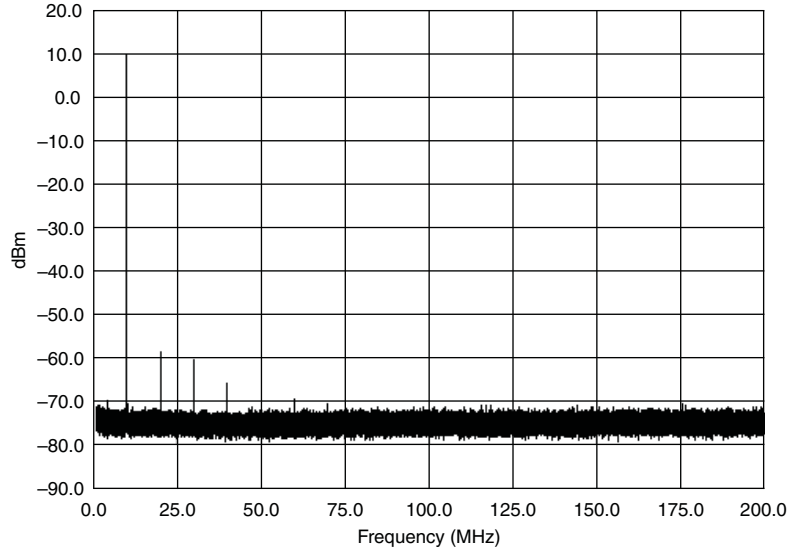
Average Noise Density		Amplitude Range		Average Noise Density			Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor. All values are typical.
	Path	Vpk-pk	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz	
	Direct	1	4.0	18	-142	-146.0	
	Main	0.06	-20.4	9	-148	-127.6	
	Main	0.1	-16.0	9	-148	-132.0	
	Main	0.4	-4.0	13	-145	-141.0	
	Main	1	4.0	18	-142	-146.0	
	Main	2	10.0	35	-136	-146.0	

Figure 4. 10 MHz Single-Tone Spectrum, Direct Path, 100 MS/s, 4x DAC Interpolation (Typical)



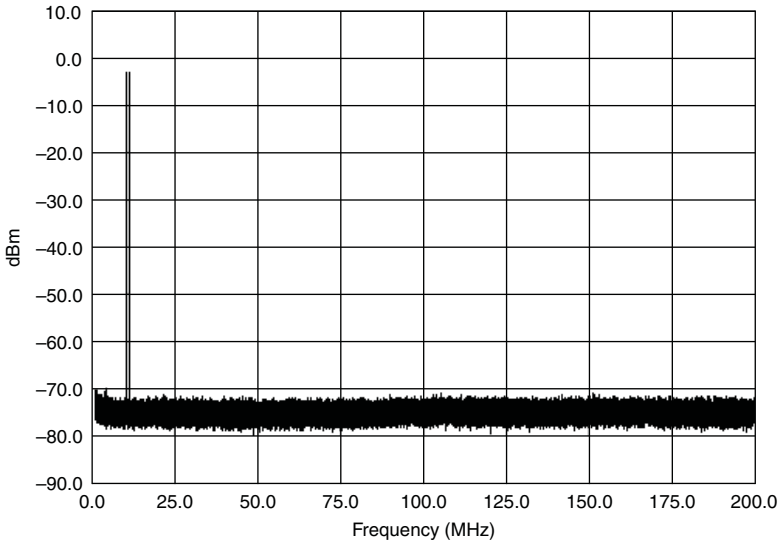
Note The noise floor in Figure 4 is limited by the measurement device. Refer to the *Average Noise Density* specifications.

Figure 5. 10 MHz Single-Tone Spectrum, Main Path, 100 MS/s, 4x DAC Interpolation (Typical)



Note The noise floor in Figure 5 is limited by the measurement device. Refer to the *Average Noise Density* specifications.

Figure 6. Direct Path, Two-Tone Spectrum (Typical)



Note The noise floor in Figure 6 is limited by the measurement device. Refer to the *Average Noise Density* specifications.

Sample Clock

Specification	Value	Comments
Sources	1. Internal, Divide-by-*N* (*N* ≥ 1) 2. Internal, DDS-based, High-Resolution 3. External, CLK IN (SMB front panel connector) 4. External, PXI star trigger (backplane connector) 5. External, PXI_Trig<0..7> (backplane connector)	Refer to the *Onboard Clock* section for more information about internal clock sources.

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td colspan="5">Sample Rate Range and Resolution</td></tr>
<tr><td>Sample Clock Source</td><td>Sample Rate Range</td><td colspan="2">Sample Rate Resolution</td><td rowspan="5">—</td></tr>
<tr><td>Divide-by-N</td><td>23.84 S/s to 100 MS/s</td><td colspan="2">Settable to (100 MS/s) / N(1 ≤ N ≤ 4,194,304)</td></tr>
<tr><td>High Resolution</td><td>10 S/s to 100 MS/s</td><td colspan="2">1.06 µHz</td></tr>
<tr><td>CLK IN</td><td>200 kS/s to 105 MS/s</td><td colspan="2" rowspan="3">Resolution determined by external clock source.
External Sample Clock duty cycle tolerance 45 to 55%.</td></tr>
<tr><td>PXI Star Trigger</td><td>10 S/s to 105 MS/s</td></tr>
<tr><td>PXI_Trig<0..7></td><td>10 S/s to 20 MS/s</td></tr>
<tr><td colspan="5">DAC Effective Sample Rate</td></tr>
<tr><td rowspan="5"></td><td>Sample Rate</td><td>DAC Interpolation Factor</td><td>Effective Sample Rate</td><td rowspan="5">DAC Effective Sample Rate = (DAC Interpolation Factor) × (Sample Rate)
Refer to the Onboard Signal Processing (OSP) section for OSP interpolation information.</td></tr>
<tr><td>10 S/s to 105 MS/s</td><td>1 (Off)</td><td>10 S/s to 105 MS/s</td></tr>
<tr><td>12.5 to 105 MS/s</td><td>2</td><td>25 to 210 MS/s</td></tr>
<tr><td>10 to 100 MS/s</td><td>4</td><td>40 to 400 MS/s</td></tr>
<tr><td>10 to 50 MS/s</td><td>8</td><td>80 to 400 MS/s</td></tr>
<tr><td colspan="5">Sample Clock Delay Range and Resolution</td></tr>
<tr><td>Sample Clock Source</td><td>Delay Adjustment Range</td><td colspan="2">Delay Adjustment Resolution</td><td rowspan="4">—</td></tr>
<tr><td>Divide-by-N</td><td>±1 Sample clock period</td><td colspan="2"><10 ps</td></tr>
<tr><td>High-Resolution</td><td>±1 Sample clock period</td><td colspan="2">Sample clock period/16,384</td></tr>
<tr><td>External (all)</td><td>0 to 7.6 ns</td><td colspan="2"><15 ps</td></tr>
</table>

Specification	Value				Comments
System Phase Noise and Jitter (10 MHz Carrier)					
Sample Clock Source	System Phase Noise Density (dBc/Hz) Offset			System Output Jitter (Integrated from 100 Hz to 100 kHz)	Specified at 2x DAC oversampling. All values are typical.
	100 Hz	1 kHz	10 kHz		
Divide-by-*N*	-110	-131	-137	<1.0 ps rms	
High-Resolution*	-114	-126	-126	<4.0 ps rms	
CLK IN	-113	-132	-135	<1.1 ps rms	
PXI Star Trigger†	-115	-118	-130	<3.0 ps rms	
External Sample Clock Input Jitter Tolerance	Cycle-cycle jitter ±300 ps Period jitter ±1 ns				All values are typical.
* High-Resolution specifications improve as the sample rate is decreased. † PXI star trigger specification is valid when the Sample clock source is locked to PXI_CLK10.					
Exported Sample Clock Destination Characteristics					
Exported Sample Clock Destinations	Characteristic				Exported Sample clocks can be divided by integer *K* ($1 \leq K \leq 4{,}194{,}304$).
	Maximum Frequency	Jitter (Typical)	Duty Cycle		
PFI <0..1> (SMB front panel connectors)	105 MHz	PFI 0: 6 ps rms PFI 1: 12 ps rms	25 to 65%		
PXI_Trig<0..6> (backplane connector)	20 MHz	—	—		

Note Sample clock purity can significantly affect the performance of an NI PXIe-5442. High amounts of jitter or phase noise in the Sample clock can create spurs in the signal generator spectrum that are not present when using a pure Sample clock. For example, if you set the Clock Mode property or the `NIFGEN_ATTR_CLOCK_MODE` attribute is set to automatic, NI-FGEN often selects

High-Resolution clocking to achieve a specific IQ rate. High-Resolution clocking has more jitter than Divide-By-*N* clocking and may create extra spurs in the signal generator output spectrum (refer to Figures 9 through 12 for examples of this phenomenon). To remove extra spurs without using software resampling, you can use a pure external clock. The NI PXI-5650/5651/5652 frequency source, with low jitter and < 1Hz frequency resolution, is an excellent option.

Onboard Clock (Internal VCXO)

Specification	Value	Comments
Clock Source	Internal Sample clocks can either be locked to a Reference clock using a phase-locked loop or be derived from the onboard voltage-controlled crystal oscillator (VCXO) frequency reference.	—
Frequency Accuracy	±25 ppm	—

Phase-Locked Loop (PLL) Reference Clock

Specification	Value	Comments
Sources	1. PXI_CLK10 (backplane connector) 2. CLK IN (SMB front panel connector)	The PLL Reference clock provides the reference frequency for the PLL.
Frequency Accuracy	When using the PLL, the frequency accuracy of the NI 5442 is solely dependent on the frequency accuracy of the PLL Reference clock source.	—
Lock Time	Typical: 70 ms Maximum: 200 ms	All values are typical.
Frequency Range	5 to 20 MHz in increments of 1 MHz. Default of 10 MHz. The PLL Reference clock frequency must be accurate to ±50 ppm.	—

Specification	Value	Comments
Duty Cycle Range	40 to 60%	—
Exported PLL Reference Clock Destinations	1. PFI <0..1> (SMB front panel connectors) 2. PXI_Trig<0..6> (backplane connector)	—

CLK IN
(Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Connector	SMB (jack)	—
Direction	Input	—
Destinations	1. Sample clock 2. PLL Reference clock	—
Frequency Range	1 MHz to 105 MHz (Sample clock destination and sine waves) 200 kHz to 105 MHz (Sample clock destination and square waves) 5 MHz to 20 MHz (PLL Reference clock destination)	—
Input Voltage Range	Sine wave: 0.65 Vpk-pk to 2.8 Vpk-pk into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 Vpk-pk to 2.8 Vpk-pk into 50 Ω	—
Maximum Input Overload	±10 V	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

PFI 0 and PFI 1
(Programmable Function Interface, Front Panel Connectors)

Specification	Value	Comments
Connectors	Two SMB (jacks)	—
Direction	Bidirectional	—
Frequency Range	DC to 105 MHz	—
As an Input (Trigger)		
Destinations	Start trigger, Script trigger	—
Maximum Input Overload	-2 V to +7 V	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
Input Impedance	1 kΩ	—
As an Output (Event)		
Sources	1. Sample clock divided by integer K ($1 \leq K \leq 4{,}194{,}304$) 2. Sample clock timebase (100 MHz) divided by integer M ($2 \leq M \leq 4{,}194{,}304$) 3. PLL Reference clock 4. Marker event 5. Data Marker event 6. Exported Start trigger 7. Exported Script trigger 8. Ready for Start event 9. Started event 10. Done event	—
Output Impedance	50 Ω	—
Maximum Output Overload	-2 V to +7 V	—

Specification	Value	Comments
V_{OH}	Minimum: 2.9 (open load), 1.4 V (50 Ω load)	Output drivers are +3.3 V TTL compatible.
V_{OL}	Maximum: 0.2 (open load), 0.2 V (50 Ω load)	
Rise/Fall Time	≤2.0 ns	Load of 10 pF.

Start Trigger

Specification	Value	Comments
Sources	1. PFI <0..1> (SMB front panel connectors) 2. PXI_Trig<0..7> (backplane connector) 3. Software 4. Immediate (does not wait for a trigger)	The Software trigger can be configured through NI-FGEN programming calls. Immediate is the default value for the Start trigger source.
Modes	1. Single 2. Continuous 3. Stepped 4. Burst	—
Edge Detection	Rising	—
Minimum Pulse Width	25 ns	Refer to the t_{s1} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Devices»NI 5442» Triggering»Trigger Timing**.

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td rowspan="5">Delay from Start Trigger to CH 0 Analog Output with OSP Disabled</td><td>DAC Interpolation Factor</td><td>Typical Delay</td><td rowspan="5">Refer to the t_{s2} documentation in the NI Signal Generators Help by navigating to NI Signal Generators Help» Devices»NI 5442» Triggering»Trigger Timing.</td></tr>
<tr><td>Digital Interpolation Filter disabled.</td><td>46 Sample clock periods + 110 ns</td></tr>
<tr><td>2</td><td>60 Sample clock periods + 110 ns</td></tr>
<tr><td>4</td><td>66 Sample clock periods + 110 ns</td></tr>
<tr><td>8</td><td>67 Sample clock periods + 110 ns</td></tr>
<tr><td>Additional Delay for Function Generator Mode</td><td colspan="2">Add 37 Sample clock periods
(Applicable to delay from Start trigger to CH 0 analog output.)</td><td>—</td></tr>
<tr><td>Additional Delay with OSP Enabled</td><td colspan="2">(29 to 120 Sample clock periods) + (0 to 40 IQ clock periods)
(Applicable to delay from Start trigger to CH 0 analog output.)</td><td>Varies with OSP configuration.</td></tr>
<tr><td colspan="4">Trigger Exporting</td></tr>
<tr><td>Exported Trigger Destinations</td><td colspan="2">A signal used as a trigger can be routed out to any destination listed in the Destinations specification of the Markers section.</td><td>—</td></tr>
</table>

Specification	Value	Comments
Exported Trigger Delay	65 ns (typical)	Refer to the t_{s3} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Devices»NI 5442» Triggering»Trigger Timing**.
Exported Trigger Pulse Width	>150 ns	Refer to the t_{s4} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Devices»NI 5442» Triggering»Trigger Timing**.

Markers

Specification	Value	Comments
Destinations	1. PFI <0..1> (SMB front panel connectors) 2. PXI_Trig<0..6> (backplane connector)	—
Quantity	One marker per segment	—
Quantum	Marker position must be placed at an integer multiple of one sample.	—
Width	>150 ns	Refer to the t_{m2} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Devices»NI 5442» Waveform Generation» Marker Events**.

Specification	Value		Comments
Skew	Destination	With Respect to Analog Output	Refer to the t_{m1} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Devices»NI 5442» Waveform Generation» Marker Events**.
	PFI <0..1>	±2 Sample clock periods	
	PXI_Trig<0..6>	±2 Sample clock periods	
Jitter	20 ps rms (typical)		—

Arbitrary Waveform Generation Mode

Specification	Value			Comments
Memory Usage	The NI 5442 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.			For more information, refer to the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Programming» Reference» NI-TClk Synchronization Help**.
Onboard Memory Size	32 MB option: 33,554,432 bytes	256 MB option: 268,435,456 bytes	512 MB option: 536,870,912 bytes	—

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Output Modes</td><td>Arbitrary Waveform</td><td colspan="2">Arbitrary Sequence</td><td>—</td></tr>
<tr><td></td><td>A single waveform is selected from the set of waveforms stored in onboard memory and generated.</td><td colspan="2">A sequence directs the NI 5442 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.</td><td></td></tr>
<tr><td rowspan="8">Minimum Waveform Size (Samples)</td><td>Trigger Mode</td><td>Arbitrary Waveform Mode</td><td>Arbitrary Sequence Mode</td><td rowspan="8">The minimum waveform size is sample rate dependent in Arbitrary Sequence mode.
For complex (IQ) data, minimum waveform size is halved.</td></tr>
<tr><td>Single</td><td>16</td><td>16</td></tr>
<tr><td rowspan="2">Continuous</td><td rowspan="2">16</td><td>96 @ >50 MS/s</td></tr>
<tr><td>32 @ ≤50 MS/s</td></tr>
<tr><td rowspan="2">Stepped</td><td rowspan="2">32</td><td>96 @ >50 MS/s</td></tr>
<tr><td>32 @ ≤50 MS/s</td></tr>
<tr><td rowspan="2">Burst</td><td rowspan="2">16</td><td>512 @ >50 MS/s</td></tr>
<tr><td>256 @ ≤50 MS/s</td></tr>
<tr><td>Loop Count</td><td colspan="3">1 to 16,777,215
Burst trigger: Unlimited</td><td>—</td></tr>
<tr><td>Quantum</td><td colspan="3">Waveform size must be an integer multiple of one sample of either real or complex (IQ) data.</td><td>—</td></tr>
</table>

Specification	Value			Comments
Memory Limits (in Samples)				
	32 MB Option	256 MB Option	512 MB Option	All trigger modes except where noted. For IQ data, maximum waveform memory is halved.
Arbitrary Waveform Mode, Maximum Waveform Memory	16,777,088	134,217,600	268,435,328	
Arbitrary Sequence Mode, Maximum Waveform Memory	16,777,008	134,217,520	268,435,200	Condition: One or two segments in a sequence. For IQ data, maximum waveform memory is halved.
Memory Limits (Continued)				
Arbitrary Sequence Mode, Maximum Waveforms	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	4,194,000 Burst trigger: 524,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Segments in a Sequence	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	6,708,000 Burst trigger: 4,180,000	Condition: Waveform memory is <4,000 (<2,000 for IQ data).

Specification	Value			Comments
Waveform Play Times				
	32 MB	256 MB	512 MB	
Maximum Play Time, Sample Rate = 100 MS/s, OSP Disabled	0.16 seconds	1.34 seconds	2.68 seconds	Single trigger mode. Play times can be significantly extended by using Continuous, Stepped, or Burst trigger modes. For IQ mode the play times are halved.
Maximum Play Time, IQ Rate = 1 MS/s, Real Mode, OSP Enabled	16 seconds	2 minutes and 14 seconds	4 minutes and 28 seconds	
Maximum Play Time, IQ Rate = 100 kS/s, Real Mode, OSP Enabled	2 minutes and 47 seconds	22 minutes and 22 seconds	44 minutes and 43 seconds	

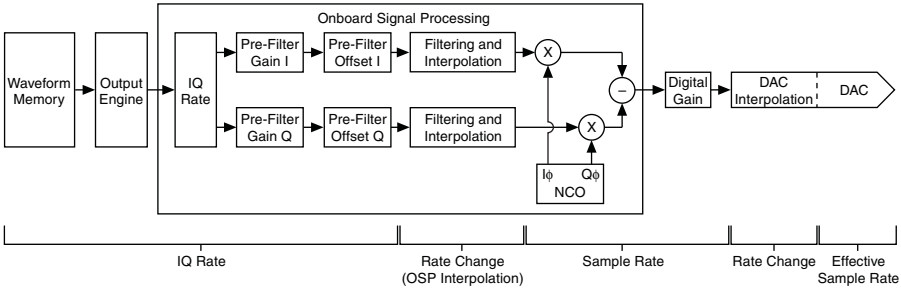
Function Generation Mode

Specification	Value		Comments
Standard Waveforms and Maximum Frequencies	Waveform	Maximum Frequency	Minimum frequency is 0 Hz for all waveforms.
	Sine	43 MHz	
	Square	25 MHz	
	Triangle	5 MHz	
	Ramp Up	5 MHz	
	Ramp Down	5 MHz	
	DC	—	
	Noise (pseudorandom)	5 MHz	
	User Defined	43 MHz	

Specification	Value	Comments
Memory Size (in Samples)	131,072 for 1/4 symmetric waveforms (Example: sine) 32,768 for non-1/4 symmetric waveforms (Example: ramp)	16-bit samples. User-defined waveforms must be exactly 32,768 samples.
Frequency Resolution	355 nHz	—
Phase Resolution	0.0055º	—

Onboard Signal Processing (OSP)

Figure 7. Onboard Signal Processing Block Diagram



Specification	Value	Comments
IQ Rate		
OSP Interpolation Range	1, 2, 4, 6, 8, 10 12 to 4,096 (multiples of 4) 4,096 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16)	Total NI PXIe-5442 interpolation = OSP interpolation × DAC interpolation
IQ Rate	Sample rate/OSP interpolation (Lower IQ rates are possible by either lowering the sample rate or doing software interpolation)	Example: For a Sample rate of 100 MS/s, IQ rate range = 6.1 kS/s to 100 MS/s

Specification	Value		Comments
Bandwidth	Real Flat	Complex Flat	Example: Complex bandwidth is 40 MHz with a complex IQ rate of 50 MS/s
	0.4 × IQ Rate	0.8 × IQ Rate	
Data Processing Modes	1. Real (I path only) 2. Complex (IQ)		—
Prefilter Gain and Offset			
Prefilter Gain and Offset Resolution	18 bits		—
Prefilter Gain Range	-2.0 to +2.0 (|Values| < 1 attenuate user data)		Unitless
Prefilter Offset Range	-1.0 to +1.0		Applied after Prefilter gain
Output	Output = (User data × Prefilter gain) + Prefilter offset(-1 ≤ output ≤ +1)		Prefilter output

Specification	Value			Comments
Finite Impulse Response (FIR) Filter Types				
Type	Parameter	Minimum	Maximum	
Flat	Passband	0.4	0.4	Lowpass filter that minimizes ripple to IQ rate × Passband.
Raised Cosine	Alpha	0.1	0.4	These filters can only be used with an OSP interpolation factor of 12 or greater.
Root Raised Cosine	Alpha	0.1	0.4	

Specification	Value	Comments
Numerically Controlled Oscillator (NCO)		
Frequency Range	1 mHz to (0.43 × sample rate)	—
Frequency Resolution	Sample rate / 2^{48}	Example: 355 nHz with a sample rate of 100 MS/s
I and Q Phase Resolution	0.0055º	—
Phase Quantization	17 bits	Look-up table address width
Tuning Speed	1 ms	—

Specification	Value		Comments
IF Modulation Performance (Typical)			
Modulation Configuration	Measurement Type	Value	Direct path (4 dBm peak), 25 MHz carrier
GSM Physical Layer*	MER (Modulation Error Ratio)	56 dB	
	EVM (Error Vector Magnitude)	<0.2% rms	
W-CDMA Physical Layer†	MER	48 dB	
	EVM	<0.4% rms	
DVB Physical Layer‡	MER	44 dB	
	EVM	<0.5% rms	
20 MSymbols/s 64 QAM**	MER	39 dB	
	EVM	<0.8% rms	
26.09 MSymbols/s 64 QAM**	MER	36 dB	
	EVM	<1.0% rms	
34.78 MSymbols/s 64 QAM**	MER	32 dB	
	EVM	<1.6% rms	

* OSP Enabled. IQ Rate = 1.083 MS/s, 4 Samples/Symbol. FIR Filter Type = Flat, Passband = 0.4, Prefilter Gain = 0.4. MSK modulation. Software Pulse Shaping and Phase Accumulation, 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 11.

† OSP Enabled. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.22, Prefilter Gain = 0.35. QPSK modulation. PN Sequence Order = 12.

‡ OSP Enabled. IQ Rate = 6.92 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.15, Prefilter Gain = 0.4. 32 QAM modulation. PN Sequence Order = 12.

** OSP Enabled. IQ Rate = 50 MS/s. FIR Filter Type = Flat, Passband=0.4, Prefilter Gain = 0.6. 64 QAM modulation. Software Pulse Shaping and Resampling, Root-Raised Cosine, Alpha = 0.15. PN Sequence Order = 15.

Specification	Value	Comments
Digital Performance		
Maximum NCO Spur	<-90 dBc	Full-scale output
Interpolating Flat Filter Passband Ripple	<0.1 dB	Passband from 0 to (0.4 × IQ rate)
Interpolating Flat Filter out of Band Suppression	>80 dB	Stopband suppression from (0.6 × IQ rate)

Figure 8. Real Interpolation Filter Frequency Response IQ Rate = 10 MS/s

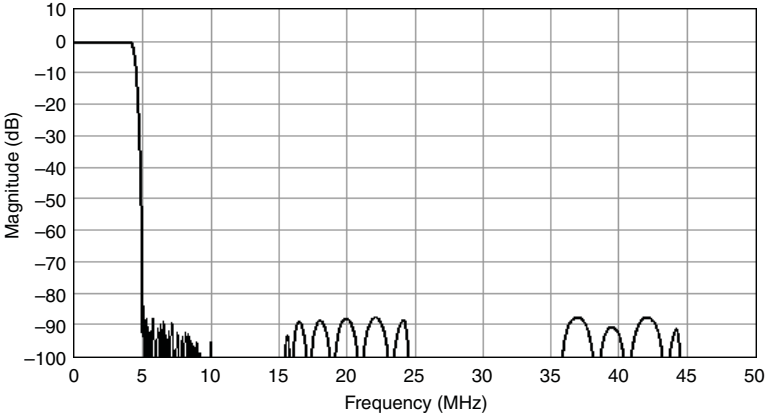


Figure 9. GSM Physical Layer[1, 2] External Sample Clocking = 99.665 MHz

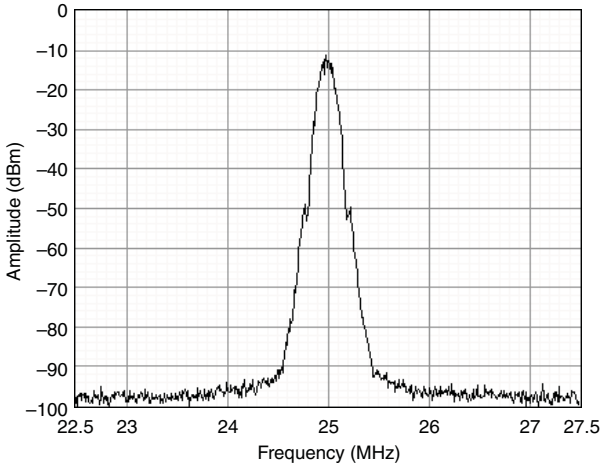
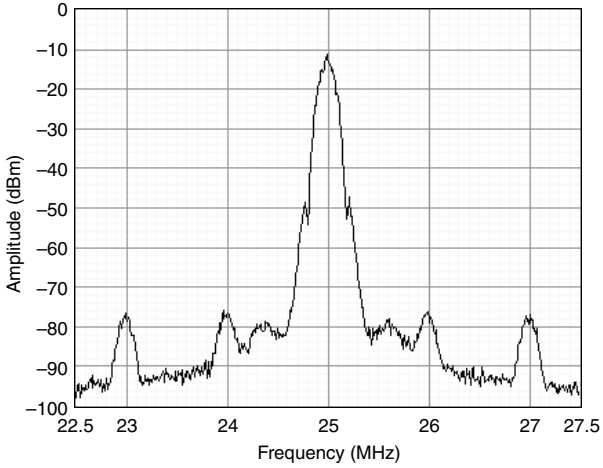


Figure 10. GSM Physical Layer [1, 2] Internal (High-Resolution) Sample Clocking = 99.665 MHz
Additional Artifacts are due to High-Resolution Clock Spurs.



[1] OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 1.083 MS/s, 4 samples/symbol. FIR Filter Type = Flat, Passband = 0.4. Software MSK modulation: 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 14.

[2] For more information about eliminating spurs, refer to the *Note* in the *Sample Clock* section.

Figure 11. DVB Physical Layer[1, 2]
External Sample Clocking = 96.88 MHz

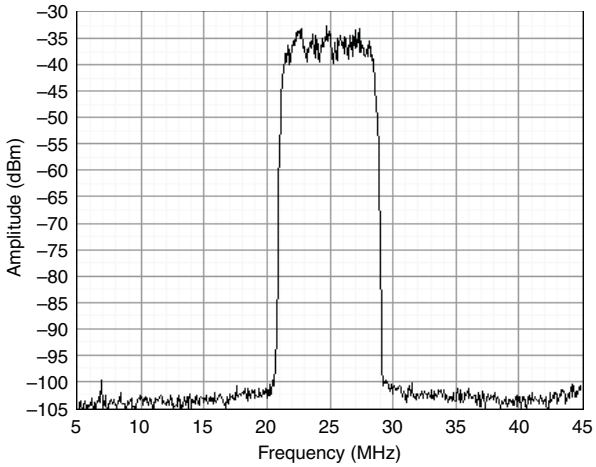
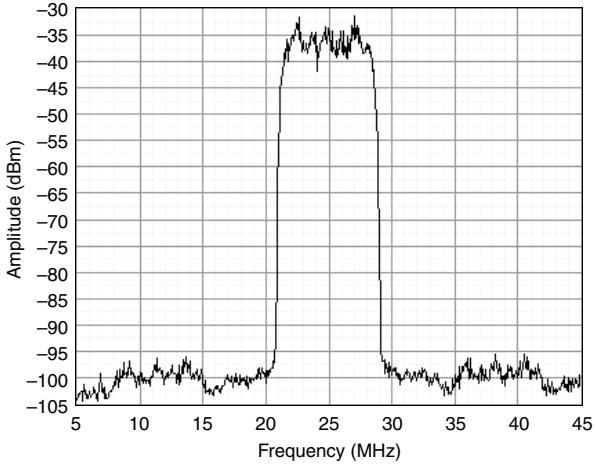


Figure 12. DVB Physical Layer[1, 2]
Internal (High-Resolution) Sample Clocking = 96.88 MHz
Additional Artifacts are due to High-Resolution Clock Spurs.



[1] OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 6.92 MS/s, 1 sample/symbol. FIR Filter Type = Root- Raised Cosine, Alpha = 0.15. 32 QAM modulation. PN Sequence Order = 15.

[2] For more information about eliminating spurs, refer to the *Note* in the *Sample Clock* section.

Figure 13. W-CDMA Physical Layer[1]
Internal (High-Resolution) Sample Clocking = 92.16 MHz

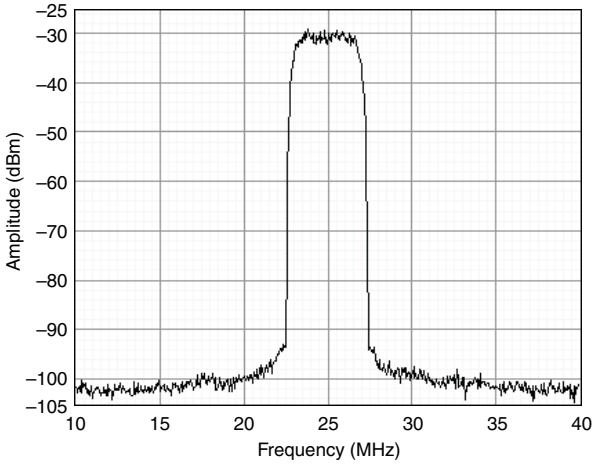
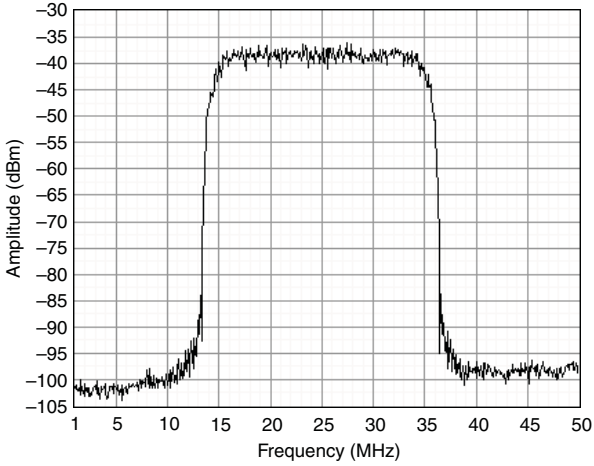


Figure 14. 20 MSymbols/s 64 QAM[2]



[1] OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root-Raised Cosine, Alpha = 0.22. QPSK modulation. PN Sequence Order = 15.

[2] OSP Enabled. Direct Path (4 dBm peak). 25 MHz Carrier. IQ Rate = 50 MHz. FIR Filter Type = Flat Passband = 0.4. Software 64 QAM modulation. Root-Raised Cosine Alpha = 0.15. PN Sequence Order = 15.

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.	—
External Calibration	The external calibration calibrates the VCXO, voltage reference, output impedance, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.	—
Calibration Interval	Specifications valid within 2 years of external calibration.	—
Warm-up Time	15 minutes	—

Power

Specification	Typical	Maximum	Comments
+3.3 VDC	1.67 A	2.0 A	—
+12 VDC	1.9 A	2.2 A	
Total Power	28.3 W	33 W	

Software

Specification	Value	Comments
Driver Software	NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5442. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C++ .NET • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Interactive Control and Configuration Software	The FGEN Soft Front Panel supports interactive control of the NI 5442. The FGEN Soft Front Panel is included on the NI-FGEN driver CDs. Measurement & Automation Explorer (MAX) provides interactive configuration and test tools for the NI 5442. MAX is also included on the NI-FGEN CDs. You can use the NI 5442 with NI SignalExpress.	—

Physical

Specification	Value	Comments
Dimensions	3U, One Slot, PXI Express module 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)	—
Weight	405 g (14.3 oz)	—

Specification	Value		Comments
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH 0	Analog output	SMB (jack)	
CLK IN	Sample clock input and PLL reference clock input	SMB (jack)	
PFI 0	Marker output, trigger input, Sample clock output, exported trigger output, and PLL Reference clock output	SMB (jack)	
PFI 1	Marker output, trigger input, Sample clock output, exported trigger output, and PLL Reference clock output	SMB (jack)	
Front Panel LED Indicators			
Label	Function		For more information, refer to the *NI Signal Generators Help*.
ACCESS	The ACCESS LED indicates the status of the PCI bus and the interface from the NI 5442 to the controller.		
ACTIVE	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5442.		
Included Cable			
	1 (NI part number 763541-01), 50 Ω, BNC Male to SMB Plug, RG223/U, Double Shielded, 1 m cable.		—

NI PXIe-5442 Environment

Note To ensure that the NI 5442 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5442 kit.

Specification	Value	Comments
Operating Temperature	0 ºC to +55 ºC in all PXI Express chassis produced by NI. Meets IEC 60068-2-1 and IEC 60068-2-2. **Note**: Refer to KnowledgeBase 4AEB2ML1 at `ni.com/support` for more information about maximizing PXIe data transfer rates when operating at ambient temperatures below 10 ºC.	—
Storage Temperature	-25 ºC to +85 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC 60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC 60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms}. Meets IEC 60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 meter maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—
Indoor use only.		

Compliance and Certifications

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility (EMC)

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions, Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。 (For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

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Visit ni.com/register to register your National Instruments product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

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